DesignCon 2008

Track 12: Test Fixturing and Measurement Methodology (12-WP2)

Characterization Methodology for High-Density Microwave Fixtures

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February 6, 2008





- Methodology for Modeling the Test Fixture
- Test Setup for Measuring the Test Fixture
- Characterization of TDR, DC, and AC fixtures





Why model?

- To build an equivalent circuit to mimic the behavior of an interconnect structure.
- This allows the structure's behavior to be:

1) understood in order to find performance limitations

- 2) used in simulations
- 3) used to create a de-embedding file if used as a fixture
- A simulation model can be built using different elements:
 - 1) Transmission Lines
 - 2) RLC components
 - 3) S-parameter blocks
 - 4) CAD specific simulation blocks (Wline, etc...)





How do we know what to model?

- The goal of a model is to match the performance of the structure.
- The performance of the structure can be obtained in a variety of ways:
 - 1) Time Domain Reflectrometry (TDR)
 2) Vector Network Analysis (VNA)
 3) EM Simulations (FEA, FD, MoM, etc...)





What technique is best?

- It is completely up to the user. Each method *should* produce the same result.
- Our approach is:
 - 1) <u>Time Domain Reflectrometry (TDR)</u>: to measure the structure's performance:
 - measurement is always preferred, requires hardware and good fixturing
 - TDR allows the spatial separation of discontinuities
 - TDR is more intuitive than S-parameters for discontinuity separation
 - 2) <u>RLC Components</u>: to build equivalent circuit model
 - RLC's are simulator agnostic
 - RLC's give a good gut feel for the magnitude of discontinuities

3) <u>Manual Modeling</u>: to match modeled performance to measurement

- more time consuming that automated techniques
- But, allows an intuitive feel to be developed





The Modeling Process

- We energize a DUT with an arbitrary stimulus (TDR or VNA)
- We observe the response of the DUT



• Since the quantities are complex, we can transform between the time and frequency domain. This allows one measurement to present information in both domains.





The Modeling Process

- x(t), X(s) is the stimulus
 - what we energize the DUT with:
 - a voltage step for TDR
 - a sine wave for a VNA
- *h(t)*, H(s) is the transfer function of the DUT
 - the equivalent circuit of the probe
- y(t), Y(s) is the output of the system
 - y(t) is what we see on the TDR oscilloscope screen
 - Y(s) is what we see on the VNA screen

NOTE: We're trying to model h(t), but we only get to observe y(t)







The Modeling Process

- We first build an accurate model of the forcing function x(t)
- This allows us to construct a simulation model of *h(t)*
- When the modeled *y(t)* matches what was measured, we have an accurate h(t) model
- Now x(t) can be changed to other sources:
 - evaluate the true performance of the DUT without stimulus imperfections
 - create performance specifications (-3dB BW, Step Response)
 - switch Domains (TDR to S-parameters)
- The same approach can be used to remove test fixture impact on system







PCI Express Probe Overview (*the DUT***)**

Summary

- connects to industry standard x16 PCI Express Gen 1 midbus footprint
- brings out signals to high-frequency SMP connectors
- Coax cables connect SMP's to test equipment
- Uses SPIRIT connector-less technology for high density interconnect

• TDR Configuration

- 50 Ω through system
- used to drive signals into the system using TDR or BERT
- can be used on dedicated Tx line to observe jitter using scope (parametric testing)

• DC Configuration

- DC coupled, 7:1 resistive divider probe
- used when measuring DC level during no activity is desired

• AC Configuration

- AC coupled, 7:1 resistive divider probe
- used when DC loading is prohibitive and bus is 100% active







Measurement Setup

TDR/TDT Based

Agilent ADS simulation tool



Tektronix DSA8200 with 80E04 18GHz TDR Module

PT100-TDR Test Fixture









Test Setup for Measuring the DUT

Test Setup

The DUT is tested as an In-Line Load.

The most straight forward method is to configure it as a 50ohm system.

In-Line Test Circuit





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Characterization (Nodes)

1) Measurement Setup and Observation Ports











Characterization (Nodes)

1) Measurement Setup and Observation Ports













Measurement Results (TDR/TDT)

1) TDR/TDT Measurements at all defined ports





Modeling (R1)

R1: Measured vs. Modeled Response of stimulus



- The source of the TDR can be captured and used as a stimulus source in SPICE using the *Vfile* element
- This allows any imperfections of the instrument to be accurately modeled in x(t)





Modeling (R2)

R2: Measured vs. Modeled Response for the test fixture



- The test fixture has a very consistent impedance, so it can be modeled using a traditional transmission line.
- Impedance of the measurement is first matched using an ideal T-line element:
- Then a lossless LC model is constructed using values calculated from:

$$Z_0 = \sqrt{\frac{L}{C}} \qquad \qquad T_D = \sqrt{LC}$$

- 10 LC segments are used to model a delay equal to the highest rise time we want to model (~10GHz or 35ps)





Modeling (R3)

R3: Measured vs. Modeled Response of DUT



- An impedance discontinuity is observed due to the high density point-of-contact interconnect.
- The TDR shows a *positive* reflection indicating an inductive discontinuity.
- An attempt is first made to model this using a single inductor. However, the length of the discontinuity cannot be modeled using a single element.
- A series of LC T-line segments are instead used to model impedance and delay.





Modeling (R3 Eq Ckt)

R3: Measured vs. Modeled Response of DUT



- Again, 10x segments per rise time (35ps in this case) are used. The
- Again, the L and C values of the lossless model are found using:

$$Z_0 = \sqrt{\frac{L}{C}} \qquad T_D = \sqrt{LC}$$



Modeling (R4)

R4: Measured vs. Modeled Response of full system with termination



- The same impedance discontinuity is observed but now the end is terminated so there are no unwanted reflections.
- The easiest way to terminate the system is into the 50ohm input of the TDR scope (i.e., the TDT path).





Modeling (R5)

R5: Measured vs. Modeled Response of TDT



- The TDT of this system has a *slow tail*, which is characteristic *frequency* dependent loss (skin effect or dielectric loss)
- A simple method to model this frequency dependant behavior is with a parallel RC ladder network.
- Each tau is selected to switch in a different shunt impedance at a different frequency. One network per decade typically can model this to the first order.





Modeling (R5 Eq Ckt)

R5: Measured vs. Modeled Response of TDT





- One ladder network is sized to model the dielectric loss in the PCB.
- Another ladder network is sized to model the skin effect loss in the cable.





Modeling (R6 & R7)

R6: Measured vs. Modeled Response "Near-End & Far-End Crosstalk"







R7 : Far-End Cross-Talk with all Ports Terminated







Modeling (R6 & R7)

R6/R7: Measured vs. Modeled Response of Cross-talk Crosstalk

- Things observed from these results:
- 1) There is distributed X-talk due to the coupled traces on the PCB
- 2) There is a near-end and far end X-talk due to the high density interconnect.

Initially this looks due to inductive coupling.

However, previously we said that the interconnect was distributed and needed to be modeled using LC segments.

This means that we will have a portion of capacitive coupling also.









X-talk Modeling

R6/R7: Measured vs. Modeled Response of Cross-talk Crosstalk

- A quick note on X-talk

- Ideal Capacitive Coupling produces Near and Far End X-talk both with equal and positive amplitudes.
- 2) Ideal Inductive Coupling produces Near and Far End X-talk with equal amplitudes but opposite polarities.

Near-End = Positive Amplitude Far-End = Negative Amplitude

Note: the high density interconnect is not in an homogenous medium so the Far-End X-talk due to L and C do not cancel.





Modeling (Eq Ckt)

Equivalent Circuit Model of SPIRIT Interconnect

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- Mutual Inductance and Capacitance values are added along the distributed circuit until the modeled response matches the measurement.





Modeling (Eq Ckt)

Equivalent Circuit Model of Fixture PCB



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Modeling (Eq Ckt)

Equivalent Circuit Model of 12" Probe Cables



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Characterization with Different Sources

Changing Sources

• Now that we have a good model of our DUT, i, we can change the source that we drive the model in order to better understand the DUT's performance:



x(t) Ideal Current Source Gaussian Step Sine waves <u>y(t)</u>

Input Impedance Realistic Step Response S-parameters





Specifications (Zin)

DUT Performance :

Input Impedance NOTE: Removing Fixture and Instrument

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Specifications (Realistic Step Response)

DUT Performance : Differential Step Response (70ps and 35ps)







Specifications (S-parameters)

Specifications : S11 and S21







DC Characterization (Nodes)

7:1 Resistive Divider Configuration





7:1 Divider Characterization

The same process is used to model and determine the DUT performance









Characterization Summary

Summary

	TDR	DC	AC
Operating Bandwidth* Operating Data Transfer Rate* Bandwidth* (f _{-3dB}) Rise time* Attenuation	DC - 4GHz DC - 2.5 Gb/s 4 GHz 88 ps 1:1 0 dB	DC - 5GHz DC - 3.125 Gb/s 5GHz 70 ps 7:1 -16.9 dB	1 MHz - 5GHz 666 kb/s - 3.125 Gb/s 5 GHz 70 ps 7:1 -16.9 dB
Single-Ended Input Impedance** Differential Input Impedance** Single-Ended Input Capacitance** Differential Input Capacitive Load*	50 Ω 100 Ω ** -	350 Ω 700 Ω 500 fF 250 fF	350 Ω 700 Ω 500 fF 250 fF

* using 12" coaxial probe cables

** assumes the PT100 is terminated into the 50 Ω inputs of the test equipment

- *** equivalent capacitance defined as a shunt capacitor to ground in a 50 Ω system
- **** equivalent capacitance defined as a capacitor between the P and N sides of a 100 Ω differential system





Summary

- A straight forward methodology for modeling was presented
 - 1) Based on TDR Measurement
 - 2) Constructed using basic RLC elements
 - 3) Used a manual process
- This approach has the advantages of:
 - 1) allowing a *gut-feel* to be developed
 - 2) a vendor agnostic model
- This approach can serve as a baseline for using automated modeling procedures on subsequent revisions





Thank you





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