13th NASA VLSI Design Symposium
Systems Session

Off-Chip Coaxial to Microstrip Transition Using MEMs Trench

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Motivation

- **Package interconnect limits performance in VLSI systems**
- **This is caused by :**

  1) Electrical parasitics of the package interconnect

  2) On-chip technology outpacing off-chip technology

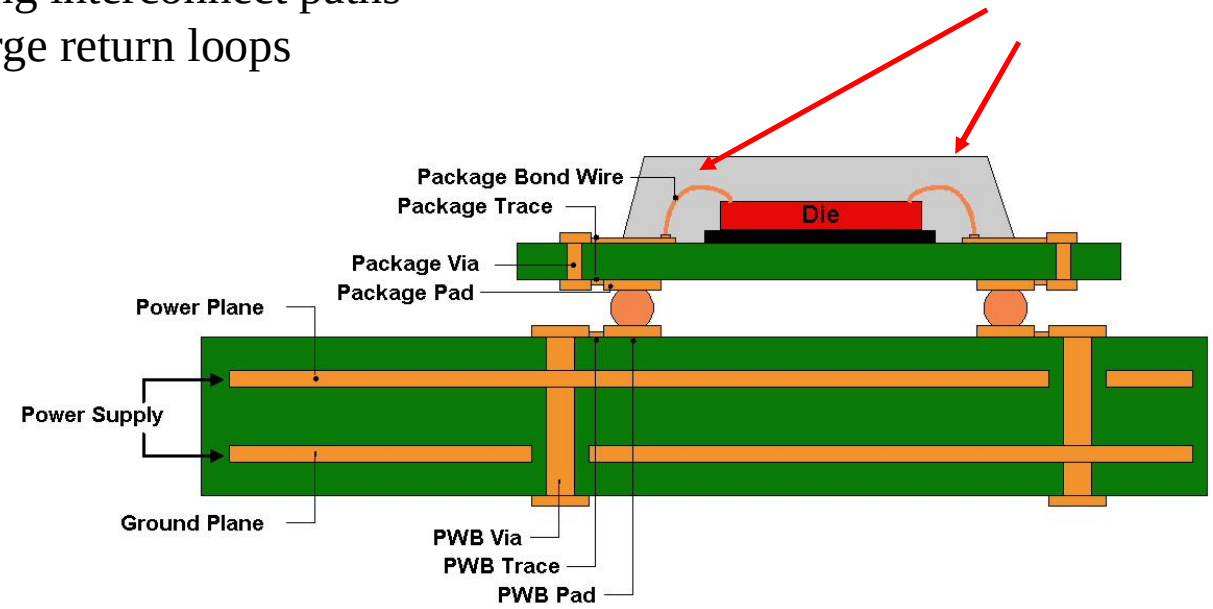
Why is packaging limiting performance?

- **Today's Package Interconnect Looks Inductive**

Wire Bond Inductance (~2.8nH)

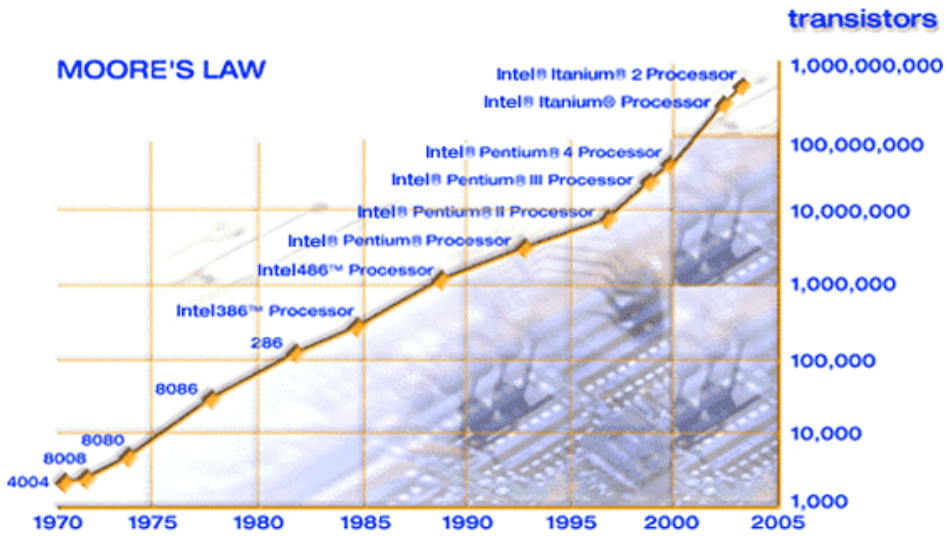
- Long interconnect paths
- Large return loops

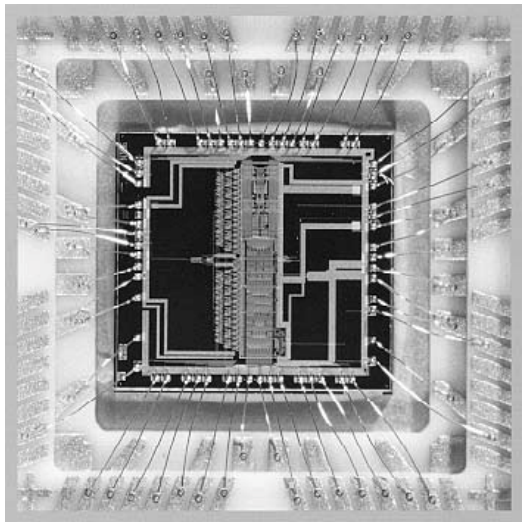
$$L = \frac{\Phi}{I}$$



- **Today's Package Impedance is Not Controlled**

Why is packaging limiting performance?





Transistor Technology is Outpacing Package Technology

Problem : Packaging Limits Performance

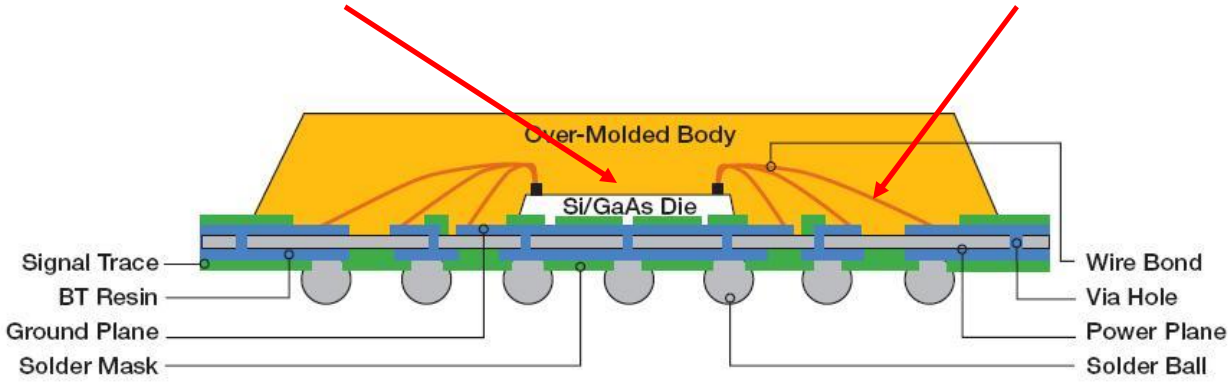
- **Transistor Technology is Faster than Package Technology**

IC

"Moore's Law"
- # of transistors will double every 18 months

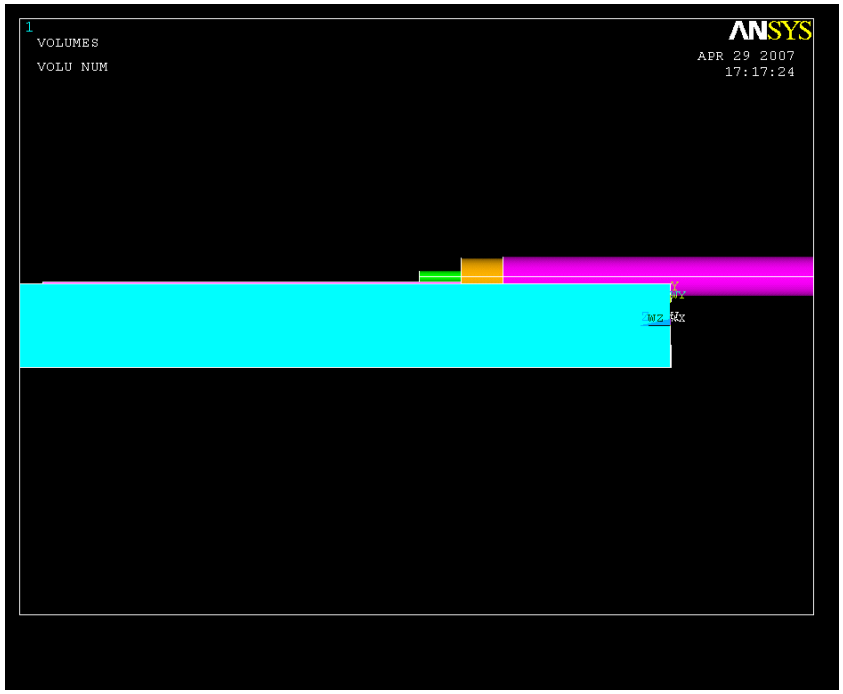
Package

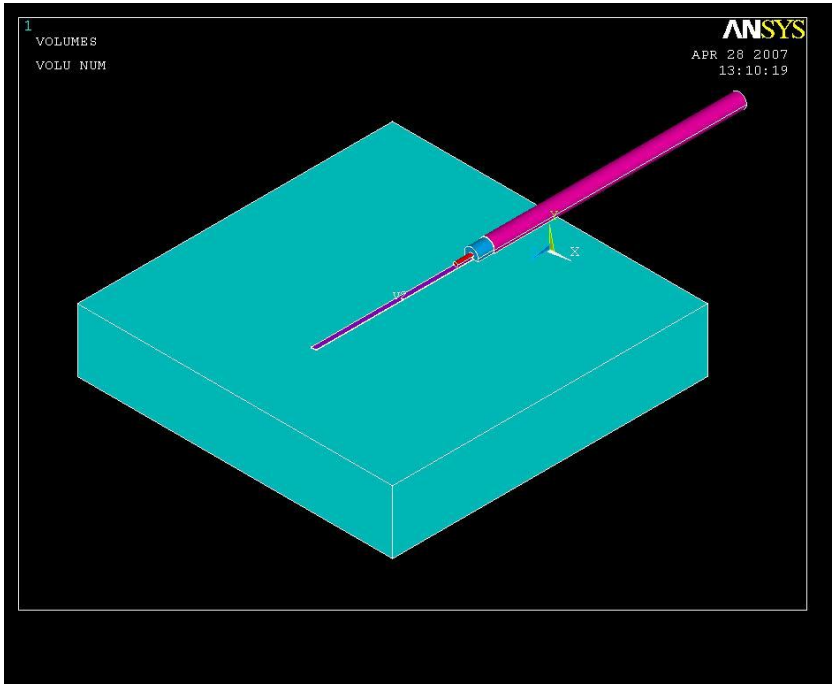
"Rent's Rule"
- # of I/O will double in next 10 years



Proposed Solutions – New Interconnect Technology

- **Coaxial to Microstrip Launch**
  - **Use MEMs process technology**
  - **Target System on Package (SoP) applications**





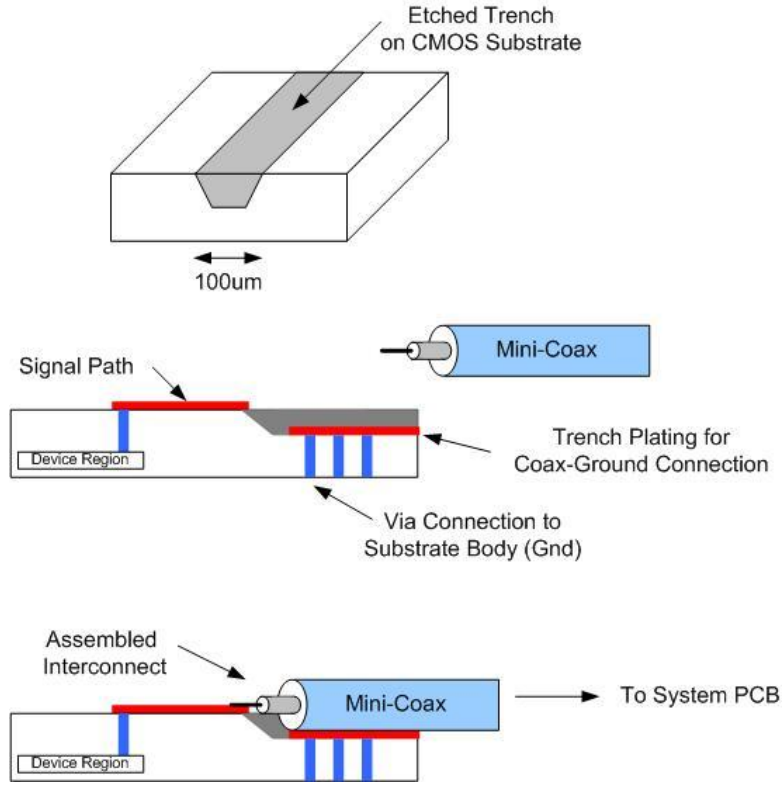
Coaxial to Microstrip Launch

- **On-Chip = Microstrip Transmission Line**

- **Off-Chip = Coaxial Transmission Line**

- **A MEMs trench is used to :**

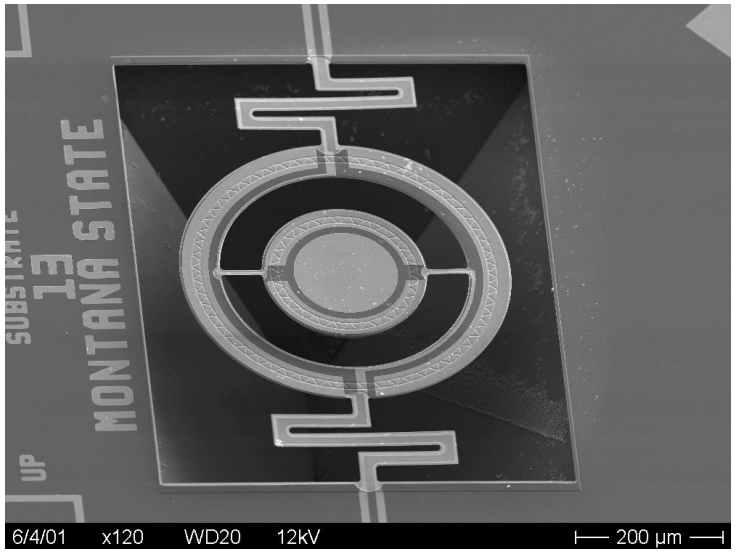
  - mechanically support the coax
  - align the conductors
  - provide return path connection



Coaxial to Microstrip Launch

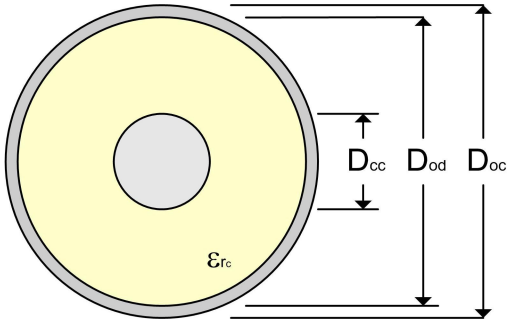
- MEMs launch achieved using standard *Etch – Growth – Release* process

- Experience with this type of process at the Montana Microfabrication Facility (MMF)



Coaxial to Microstrip Launch

Geometric Dependencies - Coax



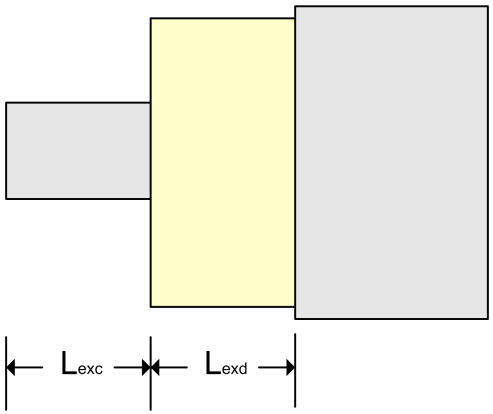
$$Z_{0_{coax}} = \frac{138}{\varepsilon_r} \cdot \log\left(\frac{D_{od}}{D_{cc}}\right)$$

- the coax inner diameter is the base dimension

- assuming a commercially available wire (42, 46, 50 AWG)

- 50Ω impedance requirement sets coaxial dimensions

- extension diameters dictated by mechanical reliability



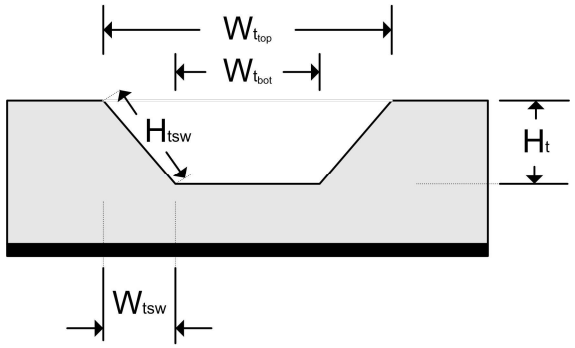
Coaxial to Microstrip Launch

Geometric Dependencies - Trench

- the trench must be wide enough to accept the coaxial outer diameter

- the depth must place the coaxial center conductor on top of the microstrip trace

- using inscribed octagonal geometries sets dimensions for trench



$$W_{t_{bot}} = D_{oc} \cdot \tan(22.5)$$

$$H_{tsw} = \frac{H_t}{\sin(45)}$$

$$W_{tsw} = \frac{H_t}{\tan(45)}$$

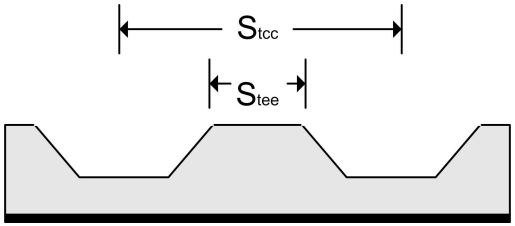
$$W_{t_{top}} = W_{t_{bot}} + 2 \cdot W_{tsw}$$

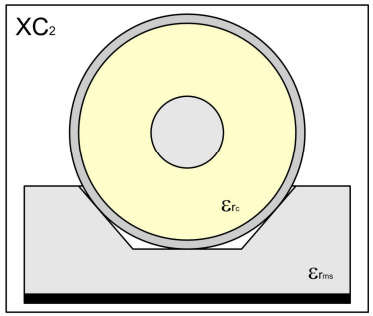
$$H_t = \left(\frac{D_{oc}}{2}\right) - \left(\frac{D_{cc}}{2}\right) - T_{ms}$$

Coaxial to Microstrip Launch

Geometric Dependencies – Channel Spacing

- spacing of adjacent trenches must accommodate coax protrusion



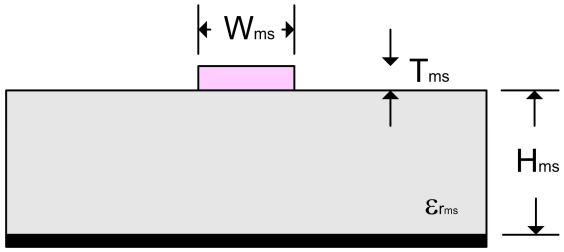


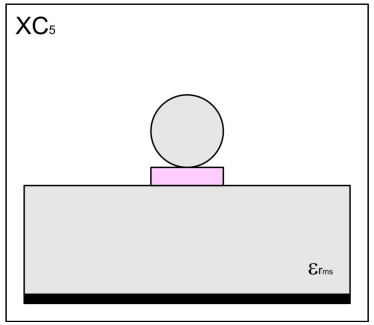
Coaxial to Microstrip Launch

Geometric Dependencies – On Chip Trace

- dimension of microstrip transmission line is dictated by :

1) 50Ω Impedance requirement
2) Height from bottom of trench to bottom of coax center conductor





$$Z_{0_{ms}} = \frac{120 \cdot \pi}{\sqrt{\varepsilon_{eff}} \cdot \left[\frac{W_{ms}}{H_{ms}} + 1.393 + \frac{2}{3} \cdot \ln\left(\frac{W_{ms}}{H_{ms}} + 1.444 \right) \right]}$$

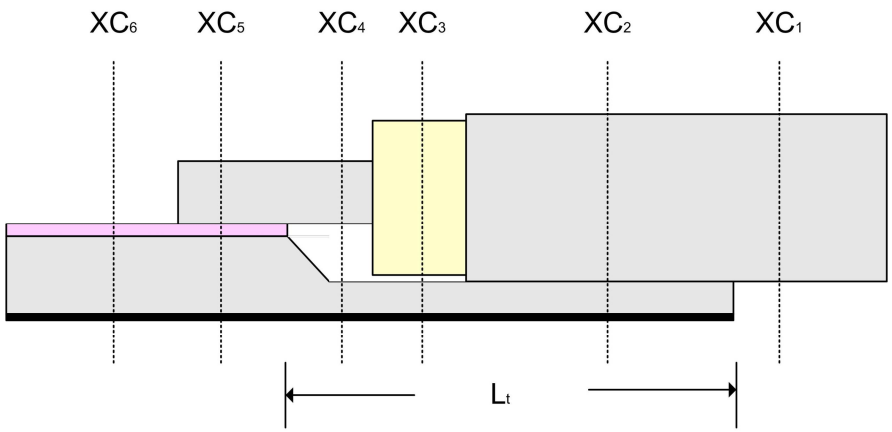
$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2 \cdot \sqrt{1 + 12 \cdot \left(\frac{H_{ms}}{W_{ms}} \right)}}$$

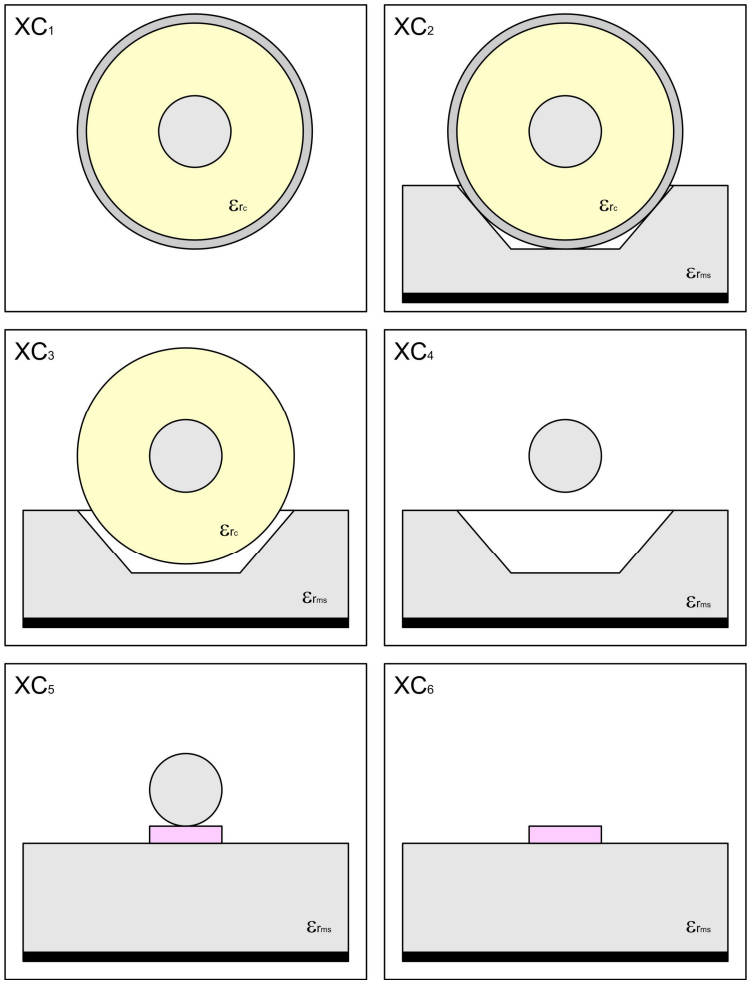
Coaxial to Microstrip Launch

Impedance Concerns

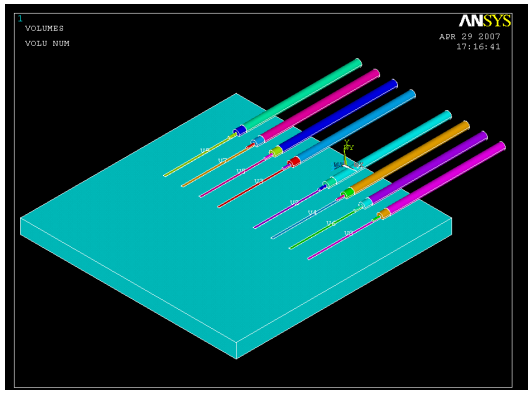
- between the coax and microstrip T-lines, there are regions of impedance discontinuities

- these should be understood but are small relative to the overall interconnect length





Coaxial to Microstrip Launch



Spatial Evaluation

- is this interconnect at least as small or smaller than current interconnect?

- we evaluate against 100μm x 100μm pad requirements for wire bond and flip-chip

Par	Units	Wire Bond	Flip Chip		Coaxial Line	
				42_{AWG}	46_{AWG}	50_{AWG}
D_{CC}	μm	-	-	64	41	25
D_{OD}	μm	-	-	214	137	84
D_{OC}	μm	-	-	230	147	90
T_{ms}	μm	-	-	10	10	10
W_{ms}	μm	-	-	64	41	25
H_{ms}	μm	-	-	41	29	20
W_{tbot}	μm	-	-	95	61	37
H_t	μm	-	-	73	43	23
H_{tsw}	μm	-	-	103	61	32
W_{tsw}	μm	-	-	73	43	23
W_{ttop}	μm	-	-	241	147	83

Results

- 42 and 46 AWG wires require more silicon area than traditional 100 μm pad (141% & 47%)

- 50 AWG wire requires **17% less area**

Coaxial to Microstrip Launch

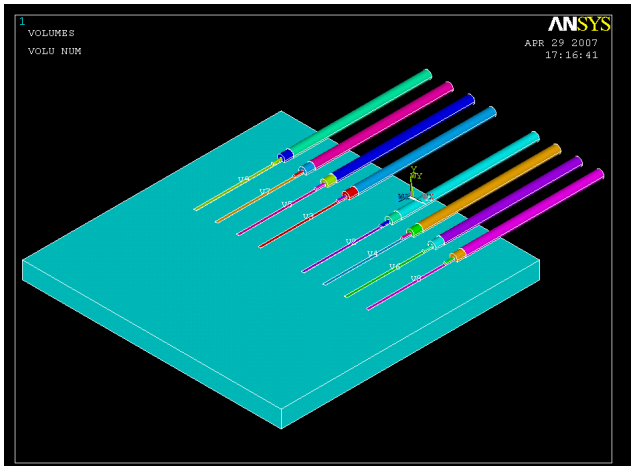
Electrical Evaluation

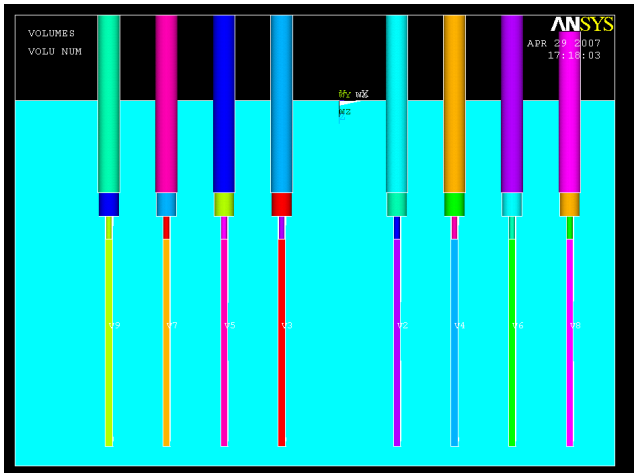
- we need to evaluate if this type of interconnect is worth pursuing electrically

- first order FEA modeling was done in *Ansys*

- results are compared to traditional SoP interconnect (wire bond and flip-chip)

- we look at unit Capacitance, Inductance, and Impedance between the different interconnect options





Coaxial to Microstrip Launch

Electrical Evaluation

- interconnect comparison
  - · coax length = 5mm
  - · wire bond length = 5mm
  - · FC bump height = 75um

Results

- versus **wire bond**:
  parasitics reduced: L → -57%
  C → -73%

- versus **flip chip**:
  parasitics higher
  Zo dropped from: 148Ω to 50Ω

Par	Units	Wire Bond	Flip Chip		Coaxial Line	
				42_{AWG}	46_{AWG}	50_{AWG}
D_{CC}	µm	-	-	64	41	25
D_{OD}	µm	-	-	214	137	84
D_{OC}	µm	-	-	230	147	90
T_{ms}	µm	-	-	10	10	10
W_{ms}	µm	-	-	64	41	25
H_{ms}	µm	-	-	41	29	20
W_{tbot}	µm	-	-	95	61	37
H_t	µm	-	-	73	43	23
H_{tsw}	µm	-	-	103	61	32
W_{tsw}	µm	-	-	73	43	23
W_{ttop}	µm	-	-	241	147	83
L'	nH/m	569	65	242	242	242
C'	pF/m	26	8	97	97	97
Zo	Ω	148	91	50	50	50
L_{5mm}	nH	2.85	0.32	1.21	1.21	1.21
C_{5mm}	pF	0.13	0.04	0.48	0.48	0.48

NOTE: first order FEA modeling was done in *Ansys*

Summary

1) A new SoP interconnect was presented and compared to current technology

- Coaxial to Microstrip launch using MEMs trench

2) Spatially this interconnect has the potential to require less perimeter area

3) Electrically this interconnect has the potential perform faster

- less parasitic L and C
- ability to control impedance

4) Next Steps

- full wave FEA
- prototype assembly and measurement

Questions?